WHAT IS CLAIMED IS:

1. A method for deriving a fractional-rate clocked logic circuit from a full-rate clocked logic circuit comprising combinatorial functions and sequential functions for operating on block input signals to produce block output signals, wherein the sequential functions operate at a full-rate clock frequency, the method comprising:

deriving combinatorial logic elements based on the combinatorial functions, each of the combinatorial logic elements responsive to a subset of the block input signals for producing combinatorial signals;

deriving sequential logic elements based on the sequential functions, each of the sequential logic elements responsive to a subset of the combinatorial signals and a fractional clock signal for producing register signals, wherein a frequency of the fractional clock signal is a fraction of the full-rate clock frequency, and wherein at least one of the sequential logic elements further produces a register feedback signal;

wherein certain of the combinatorial logic elements are each further responsive to a subset of the combinatorial signals, and wherein at least one of the combinatorial logic elements is further responsive to the register feedback signal; and

combining the register signals for producing the block output signals.

2. The method of claim 1 wherein the combinatorial logic elements are substantially identical, and wherein the sequential logic elements are substantially identical.

3. The method of claim 1 wherein each of the combinatorial logic elements implements a function F(X, Y), and wherein X and Y represent signals input to a combinatorial logic element and operated on by the function F( ).

4. The method of claim 3 wherein X comprises the subset of the block input signals, and wherein Y comprises the subset of the combinatorial signals.

5.. The method of claim 1 wherein the block input signals and the block output signals each comprise signal vectors, and wherein each signal vector further comprises a plurality of logic signals.

6. The method of claim 1 further comprising segregating the block input signals into subsets of the block input signals by assigning each block input signal to one of the subsets of the block input signals.

7. A method for deriving a half-rate clocked logic circuit from a full-rate clocked logic circuit comprising combinatorial functions and sequential functions for

operating on block input signals to produce block output signals, wherein the sequential functions operate at a full-rate clock frequency, the method comprising:

forming a first and a second plurality of input signal groups in response to the block input signals;

forming a first combinatorial function element for receiving the first plurality of input signal groups and for producing first combinatorial signals;

forming a second combinatorial function element for receiving the second plurality of input signal groups and for producing second combinatorial signals;

forming a first sequential function element for receiving the first combinatorial signals and a half-rate clock signal for producing first register signals, wherein a frequency of the half-rate clock signal is about one-half of the full-rate clock frequency;

forming a second sequential function element for receiving the second combinatorial signals and the half-rate clock signal, for producing second register signals and register feedback signals;

supplying the first combinatorial signals as an input to the second combinatorial function element;

supplying the register feedback signals as an input to the first combinatorial function element; and

combining the first and the second register signals for producing the block output signals.

8. The method of claim 7 wherein a logic function implemented by the first and the second combinatorial function elements is substantially identical to the combinatorial functions.

9. The method of claim 7 wherein a logic function implemented by the first and the second sequential function elements is substantially identical to the sequential functions.

10. The method of claim 7 wherein the block input signals comprise a serial stream of logic signals, and wherein the step of forming the first and the second plurality of input signal groups further comprises forming the first and the second plurality of input signal groups from alternating logic signals in the stream of logic signals.

11. The method of claim 10 wherein the step of forming the first and the second plurality of input signal groups further comprises deinterleaving the serial stream of logic signals to form the first and the second plurality of input signal groups.

12. The method of claim 7 wherein the first and the second combinatorial function elements implement a function F(X, Y), and wherein X and Y represent signals input to a combinatorial function element operated on by the function F( ).

13. The method of claim 7 wherein the step of combining further comprises interleaving the first and the second register signals to produce the block output signals.

14. The method of claim 7 wherein the first plurality of input signal groups and the first register signals are even numbered signals, and wherein the second plurality of input signal groups and the second register signals are odd numbered signals.

15. The method of claim 7 wherein the block input signals and the block output signals each comprise signal vectors, and wherein each signal vector further comprises a plurality of logic signals.

16. The method of claim 7 wherein each one of the first plurality of input signal groups is earlier in time than the corresponding one of the second plurality of input signal groups.

17. A method for deriving a fractional-rate clocked logic circuit from a full-rate clocked logic circuit comprising combinatorial functions and full-rate sequential functions for operating on block input signals to produce block output signals, wherein the full-rate sequential functions operate at a full-rate clock frequency, the method comprising:

determining N, the reciprocal of the fractional rate;

segregating the block input signals into N signal groups;

providing each one of the N signal groups as an input to one of N combinatorial function elements, for producing N combinatorial signals;

providing one of the N combinatorial signals as an input to one of N sequential function elements, wherein each of the N sequential function elements produces register output signals, and wherein each of the N sequential function elements is responsive to a fractional clock rate signal, and wherein a frequency of the fractional clock signal is a fraction of the full-rate clock frequency;

wherein one of the N sequential function elements produces a register feedback signal;

wherein the nth combinatorial signal from each of the N combinatorial function elements is supplied as an input to the (n+1)th combinatorial function element, wherein n is between 0 and N-1;

wherein the register feedback signal is provided as an input to a first of the N combinatorial function elements; and

combining the N register signals to form the block output signals.

18. A method for processing logic block input signals at a clock rate to produce logic block output signals, the method comprising:

forming input signal groups in response to the block input signals;

providing one of the input signal groups to one of a plurality of combinatorial function elements, wherein each combinatorial function element produces a combinatorial signal;

providing a combinatorial signal and a clock signal operative at the clock rate to one of a plurality of sequential function elements, wherein each sequential function element produces a register signal, and wherein at least one of the sequential function elements produces a register feedback signal;

further providing a combinatorial signal to certain ones of the plurality of combinatorial function elements;

providing the register feedback signal to at least one of the plurality of combinatorial function elements; and

combining the register signals for producing the block output signals.

19. The method of claim 18 wherein the step of forming the input signal groups comprises alternatingly segregating the block input signals into one of the input signal groups.

20. The method of claim 18 wherein the step of combining the register signals comprises alternatingly combining the register signals for producing the block output signals.

21. A logic block for processing input signals and for producing output signals, comprising:

a deinterleaver for receiving and deinterleaving the input signals into a plurality of input signal groups;

a plurality of combinatorial function elements each one for receiving one of the plurality of input signal groups and for producing a combinatorial signal;

a plurality of sequential function elements each one for receiving a combinatorial signal group and a clock signal and for producing a register signal, wherein at least one of the plurality of sequential function elements produces a register feedback signal;

wherein each one of the plurality of combinatorial function elements further receives one of the combinatorial signals, and wherein at least one of the plurality of combinatorial function elements receives the register feedback signal;

an interleaver responsive to the register signals for producing the output signals.

22. A logic block for processing input signals and for producing output signals, comprising:

a deinterleaver for receiving and deinterleaving the input signals into alternating even and odd input signals;

an even combinatorial function element for receiving the even input signals and for producing even combinatorial signals;

an odd combinatorial function element for receiving the odd input signals and for producing odd combinatorial signals;

an even sequential function element for receiving the even combinatorial signals and a clock signal for producing even register signals;

an odd sequential function element for receiving the odd combinatorial signals and a clock signal for producing odd register signals and register feedback signals;

wherein the odd register feedback signals are supplied as an input to the even combinatorial function element;

wherein the even combinatorial signals are supplied as an input to the odd combinatorial function element;

an interleaver for receiving the even and odd register signals for producing the output signals.

23. A logic block for processing input signals and for producing output signals, comprising:

a deinterleaver for receiving and deinterleaving the input signals into alternating even and odd input signals;

a first even combinatorial function element for receiving the even input signals and for producing first even combinatorial signals;

a first odd combinatorial function element for receiving the odd input signals and for producing first odd combinatorial signals;

a first odd sequential function element for receiving the first odd combinatorial signals and a clock signal, for producing first odd register signals and first odd register feedback signals;

wherein the first odd register feedback signals are supplied as an input to the first even combinatorial function element;

wherein the first even combinatorial signals are supplied as an input to the first odd combinatorial function element;

a second even combinatorial function element for receiving the first odd register signals and for producing even block output signals;

a second odd combinatorial function element for receiving the first even combinatorial signals and the even block output signals and for producing second odd combinatorial signals;

a second odd sequential function responsive to the second odd combinatorial signals and the clock signal for producing odd block signals and second odd register feedback signals;

wherein the second odd register feedback signals are supplied as an input to the second even combinatorial function;

an interleaver for receiving the even and odd block signals for producing the output signals.